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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/661,281	09/14/2000	Noboru Mohri	43890-439	6246

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EXAMINER	
PATEL, ISHWARBHAI B	
ART UNIT	PAPER NUMBER
2841	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/24/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	09/661,281	MOHRI ET AL.	
	Examiner	Art Unit	
	Ishwar (I. B.) Patel	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 October 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *33,34 and 36-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *33,34 and 36-43* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 May 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/041,666.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to the amendment filed on October 26, 2006.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

3. Claims 33-34 and 36-42 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 33, the phrase "if the circuit substrate is mounted on a second substrate, the second surface is the surface mounted to the second substrate" is indefinite. The substrate can be mounted between the two substrates and in that situation any of the surface can be considered as the surface mounted to the second substrate, making it unclear in deciding the surface with larger roughness.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 33-34, 36-40 and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hamzehdoost (US Patent No. 5,689,091) in view of Muyshondt (US Patent No. 5,646,368).

Regarding claim 33, Hamzehdoost, in figure 1-4, discloses a circuit substrate comprising: a substrate (10) including a first surface and a second surface opposite to the first surface (upper and lower surface of the substrate 10);
a first conductor pattern formed on the first surface (see figure 2a); and a second conductor pattern formed on the second surface (see figure 2a). Hamzehdoost does not disclose the second surface has larger surface roughness than the first surface.

Muyshondt discloses a circuit board and recites that one circuit pattern can be formed on a copper laminated insulated sheet and the other on a build up layer can be formed by surface laminating the insulating layer on top of the other with the surface of the insulating layer roughened to provide a capability of adhering copper to that surface. This implies that the surface insulation layer with copper lamination does not need any roughening, but the surface on which the patterns are formed by plating needs the roughened surface. In other words, the roughness of the surface on one side is greater than that on the other side, depending upon the method of manufacturing the circuit board. Also, as the circuit pattern on the other side is made by plating the copper layer, a thinner layer can be plated, resulting in the saving of the copper lost in etching and facilitating production finer circuit patterns.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicants invention to provide the circuit board of Hamzehdoost with the

second surface having larger surface roughness than the first surface, as taught by Muyshondt, in order to provide better adhesive strength and help to reduce the loss of copper lost in etching and to facilitate production of finer circuit patterns.

Regarding claim 34, the modified board of Hamzehdoost further discloses an external terminal formed on the second conductor pattern (44 formed on second conductor pattern).

Regarding claim 36, the modified board of Hamzehdoost further discloses the external a ball-shaped solder (44 formed on second conductor pattern).

Regarding claim 37, the modified board of Hamzehdoost further discloses a through hole in the substrate connecting the first and second surface ((16).

Regarding claim 38, the modified board of Hamzehdoost further discloses an electrode filled in the through hole (plating along the hole 16).

Regarding claim 39, the modified board of Hamzehdoost further discloses an electrode formed along the through hole (plating along the hole 16).

Regarding claim 40, the modified board of Hamzehdoost further discloses the external terminal is connected directly underneath the electrode (44 connected to electrode on the second surface of the pattern).

Regarding claim 43, the modified board of Hamzehdoost further discloses a dielectric layer (24b) formed on at least a portion of the second conductor patterns; and a third conductor pattern formed on the dielectric layer (see figure 3a).

6. Claims 33-34, 36-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bitaillou (US Patent No. 4,830,264) in view of Komorita (US Patent No. 5,672,848)

Regarding claim 33, Bitaillou, in figure 3, discloses a circuit substrate comprising: a substrate (11) including a first surface and a second surface opposite to the first surface (upper and lower surface of the substrate 11);
a first conductor pattern formed on the first surface (see figure 3); and a second conductor pattern formed on the second surface (see figure 3). Bitaillou does not disclose the second surface has larger surface roughness than the first surface. However, the roughness on both the surface will depend upon the method of providing the pattern on the surfaces. If direct bonding of a metal plate is used the roughness requirement will be different than that for screen-printing method. Further both the direct bonding method and the screen-printing are known in the art. Komorita discloses a ceramic circuit board with both the alternative method of forming pattern by direct

bonding method and screen printing method to have the desired pattern size and fineness.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide the circuit board of Bitaillou with surface roughness suitable for either direct bonding process or screen printing method on any of the surfaces, as the first and second surfaces are relative terms to identity the surfaces, as taught by Komorita, in order to have the circuit pattern with desired size and fineness.

Regarding claim 34, the modified board of Bitaillou further discloses an external terminal formed on the second conductor pattern (22, see figure 3).

Regarding claim 36, the modified board of Bitaillou further discloses the external a ball-shaped solder (22, see figure 3).

Regarding claim 37, the modified board of Bitaillou further discloses a through hole in the substrate connecting the first and second surface (see figure 3).

Regarding claim 38, the modified board of Bitaillou further discloses an electrode filled in the through hole (19, see figure 2A).

Regarding claim 39, the modified board of Bitaillou further discloses an electrode formed along the through hole (18, figure 2A).

Regarding claim 40, the modified board of Bitaillou further discloses the external terminal is connected directly underneath the electrode (see figure 3).

Regarding claim 41, the modified board of Bitaillou further discloses a solder filled in the through hole (19, figure 2a).

Regarding claim 42, the modified board of Bitaillou discloses all the features of the claimed invention as applied to claim 41 above, but does not explicitly discloses the solder has a higher melting point than the external terminal. However, it can be seen from the figure the terminal 22 will be used to connect the board with other substrate by reflowing the solder ball 22 and the melting temperature of the solder in the hole has to be higher than that of the solder ball, other wise the solder in the holes will melt and cause short circuit on the connecting board.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide the modified board or Bitaillou with the solder having a higher melting point than the external terminal, in order to avoid melting of the solder causing short circuit on the connecting board.

Response to Arguments

7. Applicant's arguments with respect to claims have been considered but are moot in view of the new ground(s) of rejection.

Further, the applicant's arguments about the rejection with the prior art of Hamzehdoost (primary reference) and Muyshondt (secondary reference) reviewed carefully but not found persuasive. Applicant argues that Muyshondt discloses the surface roughness of the surface on one side is greater than that on the other side. But fails to disclose which side of the surface of the substrate is mounted when a circuit substrate is mounted on another substrate. First, the first surface and second surface of the substrates are relative terms for identification. Any side can be a first surface and the other will be the second surface. Further, applicant argues that there is no objective reason on the record to combine the teachings of the cited prior art. This is not found persuasive. As the patterns obtained by build up process with fine (with the narrower width). Therefore, the surface were fine line pattern is required will be formed by build up process.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Bhatt (US Patent No. 5,557,844) discloses a circuit board with the plated via holes filled with electrode material and a terminal formed directly below the electrode material.

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ishwar (I. B.) Patel whose telephone number is (571) 272 1933. The examiner can normally be reached on M-F (8:30 - 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dean Reichard can be reached on (571) 272 1984. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

IB Patel

ibp
January 21, 2007

Ishwar (I. B.) Patel
Primary Examiner